

REMARKS

The Abstract of the Disclosure has been replaced by a new Abstract which is consistent with the method of claim 8 and the methods of claims 13 and 14 for producing circuit boards using the ternary solder alloy as either a solder paste or stationery wave of liquid solder. Accordingly, the Abstract is now believed to contain sufficient details to satisfy the requirements of 37 CFR 1.72 and MPEP § 608.01(b) and the objection thereto should be withdrawn.

The rejection of claim 9 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention is respectfully traversed. Claim 9 has been amended to overcome this rejection. Accordingly, the rejection under 35 USC 112 should be withdrawn.

Applicant acknowledges the rejection of claims 8-10, 13 and 14 under the judicially created doctrine of obviousness-type double patenting over claims 12-17 of U.S. Patent No. 5,730,932 to Sarkhel, et al. If acceptable, applicant will file a Terminal Disclaimer to overcome this rejection.

The rejection of claims 8, 9, 13 and 14 under 35 USC 103 as being unpatentable over U.S. Patent 5,439,639 to Vianco in view of U.S. Patent Re. 33197 to D'Ambrosio, U.S. Patent Re. 32982 to O'Rourke or U.S. Patent 5,361,969 to Gilletta is respectfully traversed.

Applicant has amended claims 8, 13 and 14 limiting the invention to the preferred alloys exemplified by alloys 4, 5 and 6 as set forth in the specification which have melting points close to the melting point of the standard eutectic solder 63Sn/37Pb. It should be understood that the method of the subject invention permits the joining of at least two microelectronic components to one another using a ternary solder alloy

composition having the properties of the conventional tin/lead alloy composition and a high degree of ductility for the purpose of arresting crack propagation and for enhanced resistance to thermal fatigue. The method of the present invention uses a composition consisting essentially of a major proportion of tin, between 6 to about 15 weight percent bismuth and 2 to 5 wt% silver. The method as taught in claims 8 through 14 is not disclosed in any of the references cited by the Examiner and possesses a melting point close to the melting point of the standard eutectic solder.

There are a great many solder alloy compositions known in the prior art both binary and ternary compositions resulting in a very crowded field. For the Examiner merely to identify a reference teaching a ternary alloy of tin, silver and bismuth which does not meet the specified range taught by applicant is not consistent with 35 USC 103. The burden of proof is upon the Examiner to show that it is obvious to one skilled in the art to combine the references without using applicant's application as a template. The Vianco reference cited by the Examiner does not teach the claimed composition of tin, silver, bismuth as set forth in the method of the present invention nor does it disclose the wave soldering setup. Instead the cited Vianco reference teaches an alloy composition limited to 5 wt% bismuth despite the example in the table of 6.2 wt% bismuth. In fact, the last alloy in the table which has the reported 6.2 wt% bismuth content is outside the acceptable limit for bismuth as set forth in column 7, lines 20 to 24 of Vianco. Moreover, Vianco also requires the ratio of silver to tin to be about 0.036 which is another requirement which is not applicable to the method of the present invention. Accordingly, Vianco does not teach a solder composition which satisfies the requirements of the claims of the present invention. In addition, Vianco does not teach a specific wave soldering method as taught in the method of the present invention. This is in fact acknowledged by the Examiner on page 2 of the official action. There is nothing in the other cited references which would motivate one to combine those references with Vianco other than by applicant's specification. This is not a basis for combining references. For all of the

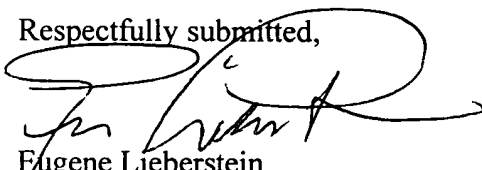
above reasons, claims 8-9 and 13-14 as amended are clearly patentable over the cited references.

The rejection of claim 10 under 35 USC 103(a) as being unpatentable over the references cited with regard to the rejection of claims 8-9 and claims 13-14 and further in view of Kattner, et al is respectfully traversed. Kattner, et al does not teach the specific range of bismuth, as taught in claim 10. In fact even if arguendo the argument of the Examiner was used, the Examiner must also show how the range in claim 10 is realized. Optimization cannot be based upon applicant's specification to support the argument.

For all of the above reasons, claims 8-10 and 13-14 are clearly patentable over the references of record.

Reconsideration and allowance of claims 8-10 and 13-14 is respectfully solicited.

Respectfully submitted,


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MAILING CERTIFICATE

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ABSTRACT OF THE INVENTION

A [high strength] method of joining two microelectronic components using
a ternary lead-free solder alloy[, solder paste and method. The alloy] which consists
essentially of a major portion of tin, from [in excess of 5] 6 wt% to about 15 wt%
bismuth [to 25 wt% bismuth] and from 2 to 5 wt% silver. The method also produces
circuit boards using the ternary solder alloy from either a solder paste or stationary wave
of liquid solder.

AMENDMENTS TO THE CLAIMS

8. (Amended) A method of joining at least two microelectronic components to one another comprising the steps of connecting the components to be joined with a ternary solder alloy consisting essentially of a major proportion of tin, between [about 5 to 25] 6 to about 15 wt % bismuth and 2 to 5 wt% silver.

9. (Amended) A method as defined in claim 8 wherein said solder alloy consists essentially of from about 70 to less than 91 weight percent tin[, from about 5 to 25 wt% bismuth and from 2 to 5 wt% silver].

13. (Amended) A process for producing circuit boards, comprising the steps of:

producing plated through holes in a circuit board;

inserting the pins of pin-in-hole components into the plated through holes;

producing a stationary wave of liquid solder consisting essentially of a major proportion of tin, between [about 5 to 25] 6 to about 15 wt% bismuth and from 2 to 5 wt% silver;

moving the circuit board across the wave with the bottom of the circuit board in contact with the wave, thereby substantially filling the plated through holes with solder;

cooling the circuit board to form solid solder joints.

14. (Amended) A process for producing circuit boards comprising the steps of:

producing a substrate with multiple wiring layers including exposed metal pads on a surface;

forming a solder paste comprising a flux, an organic vehicle and particles of metal consisting essentially of a major proportion of tin, bismuth in excess of [5] 6 wt% and up to [25] about 15 wt% and from 2 to 5 wt% silver;

depositing the solder past upon said substrate;

placing terminals of a surface mount component onto corresponding pads of the substrate;

heating said solder paste to a temperature sufficient to reflow the solder paste to connect the substrate; and

cooling to solidify the connections.

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